What is claimed is:

1. A memory cell, comprising:

a transistor having a floating channel body; and

a node to connect a drain of the transistor to a word line, said channel body having a potential which is determined based on a voltage state of the word line.

2. The memory cell of claim 1, wherein said potential corresponds to a first data value when the word line and a gate of the transistor is in a first voltage state and a source of the transistor is in a second voltage state.

3. The memory cell of claim 2, wherein the first voltage state of the word line causes impact ionization current to flow from an area near the drain to the channel body to create said potential.

4. The memory cell of claim 2, wherein the first data value is a digital one.

5. The memory cell of claim 2, wherein said potential changes to a second data value when the word line and gate assume the second voltage state and the source assumes a third voltage state.

6. The memory cell of claim 5, wherein forward bias current flows from the channel body to the source to create said potential corresponding to the second data value when the word line and gate assume the second voltage state and the source assumes a third voltage state.

7. The memory cell of claim 5, wherein the word line and gate assume different voltages values when in the second voltage state.

8. A memory cell, comprising:

a transistor having a floating channel body;

a first node to connect a source of the transistor to a bit line;

a second node to connect a gate of the transistor to a first word line;

a third node to connect a drain of the transistor to a second word line,

wherein the channel body has a potential which is determined based on voltages of the bit line and first and second word lines, said potential corresponding to a data value stored in the cell.

9. The memory cell of claim 8, wherein said potential corresponds to a first data value when the first and second word lines assume a first voltage state and the bit line assumes a second voltage state.

10. The memory cell of claim 9, wherein the first voltage state of the first word line generates capacitive coupling between the gate and channel body and the first voltage state of the second word line causes impact ionization current to flow from an area near the drain into the channel body to create said potential corresponding to the first data value.

11. The memory cell of claim 9, wherein the first voltage state is greater than the second voltage state.

12. The memory cell of claim 9, wherein the first data value is a digital one.

13. The memory cell of claim 9, wherein said potential changes to a second data value when the first and second word lines assume a second voltage state and the bit line assumes a third voltage state.

14. The memory cell of claim 13, wherein the third voltage state generates forward bias current which flows from the channel body to the source to create said potential corresponding to the second data value.

15. The memory cell of claim 13, wherein, in the second voltage state, the first word line assumes a voltage different from the second word line.

16. The memory cell of claim 13, wherein, in the second voltage state, the first and second word lines assume substantially the same voltage.

17. The memory cell of claim 13, wherein the second data value is a digital zero.

18. A method for controlling a memory cell which includes a transistor having a floating channel body, a first node connecting a source of the transistor to a bit line, a second node connecting a gate of the transistor to a first word line, and a third node connecting a drain of the transistor to a second word line, said method comprising:

setting the first and second word lines to a first voltage state; and

setting the bit line to a second voltage state, wherein the channel body assumes a potential determined by the first and second voltage states, said potential corresponding to a first data value stored in the cell.

19. The method of claim 18, wherein capacitive coupling is generated between the gate and channel body when the first word line assumes the first voltage state, and wherein impact ionization current flow from an area near the drain into the channel body to create said potential when the second word line assumes the first voltage state.

20. The method of claim 19, wherein the first data value is a digital one.

21. The method of claim 19, further comprising:

setting the first and second word lines to the second voltage state; and

setting the bit line to a third voltage state, wherein said potential changes to a second data value the first and second word lines assume the second voltage state and the bit line assumes the third voltage state.

22. The method of claim 21, wherein the third voltage state generates forward bias current which flows from the channel body to the source to create said potential corresponding to the second data value.

23. The method of claim 21, wherein, in the second voltage state, the first word line assumes a voltage different from the second word line.

24. The method of claim 21, wherein, in the second voltage state, the first and second word lines assume substantially the same voltage.

25. The method of claim 21, wherein the second data value is a digital zero.

26. A method for controlling a memory having at least first and second cells, each of said cells including a transistor having a floating channel body, a first node connecting a source of the transistor to a different bit line, a second node connecting a gate of the transistor to a first common

word line, and a third node connecting a drain of the transistor to a second common word line, said method comprising:

setting the first and second common word lines to a first voltage state; and

setting the bit lines to a second voltage state, wherein the channel bodies in the first and second cell transistors assume a potential determined by the first and second voltage states, said potential corresponding to a first data value.

27. The method of claim 26, further comprising:

changing the first and second common word lines to the second voltage state; and

changing the bit line connected to the first cell transistor to a third voltage state while maintaining the bit line of the second cell transistor at the second voltage state, wherein the channel body of the first cell transistor changes to a potential which corresponds to a second data value as a result of said changes.

28. The method of claim 27, wherein the first data value is a digital one and the second data value is a digital zero.

29. A system, comprising:

a processor; and

a memory cell including:

(a) a transistor having a floating channel body;

(b) a first node to connect a source of the transistor to a bit line;

(c) a second node to connect a gate of the transistor to a first word line;

(d) a third node to connect a drain of the transistor to a second word line, wherein the channel body has a potential which is determined based on voltages of the bit line and first and second word lines, said potential corresponding to a data value controlled by the processor.

30. The system of claim 29, wherein the processor and memory cell are located on a same chip.